**Introduction**

The main objective of this Lab session is to grasp the basic concepts of traditional Logic Circuit design using standard ICs circuits. The understanding of the electrical and timing aspects of digital devices is as well an objective of this Lab session.

**Situation given.**

The digital circuit to de realized is for a Tank System with two pumps P1 and P2 (Only P1 is being taken into account during this Session) and four sensors.

The functioning of the Pumps is dependent of certain cases.

**Lab Task 1.**

During the preparation the Boolean equation for the combinational logic of the tank controller is derived matching the cases described in the Lab Sheet.

To realize the circuit we have only used NAND gates

**-------------------------------------------------------**

Space for circuit schematic

**---------------------------------------------------------**

Truth table

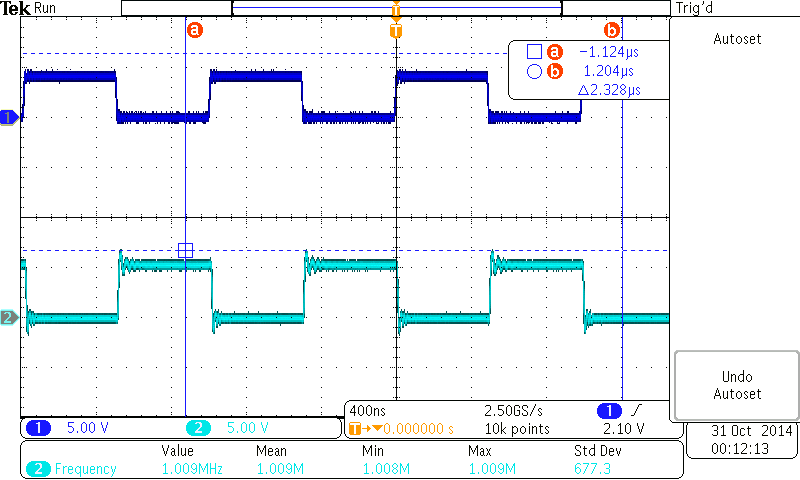
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **U** | **L** | **S1** | **Out1** | **Out2** | **P1** |
| **0** | **0** | **0** | **1** | **0** | **1** |
| **0** | **0** | **1** | **0** | **0** | **1** |
| **0** | **1** | **0** | **1** | **1** | **0** |
| **0** | **1** | **1** | **0** | **1** | **1** |
| **1** | **0** | **0** | **1** | **1** | **0** |
| **1** | **0** | **1** | **1** | **1** | **0** |
| **1** | **1** | **0** | **1** | **1** | **0** |
| **1** | **1** | **1** | **1** | **1** | **0** |

We have to convert equation to, because all operands should be NAND:

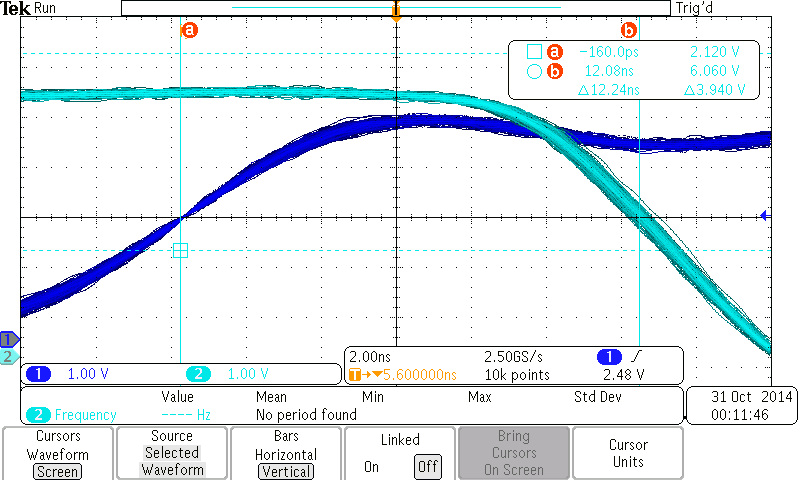
**=**

**Lab Task 2**

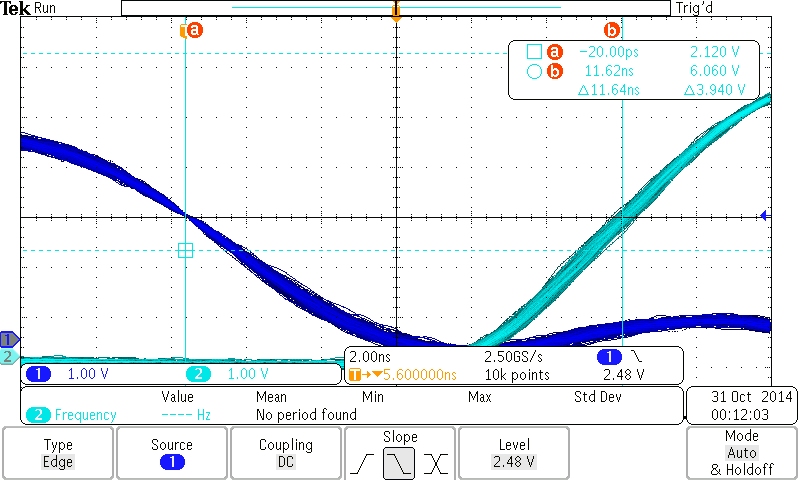
Graph shows that rectangular voltage does not exceed the range 0…5V.



The propagation delay for rising signal is 12.24 ns.

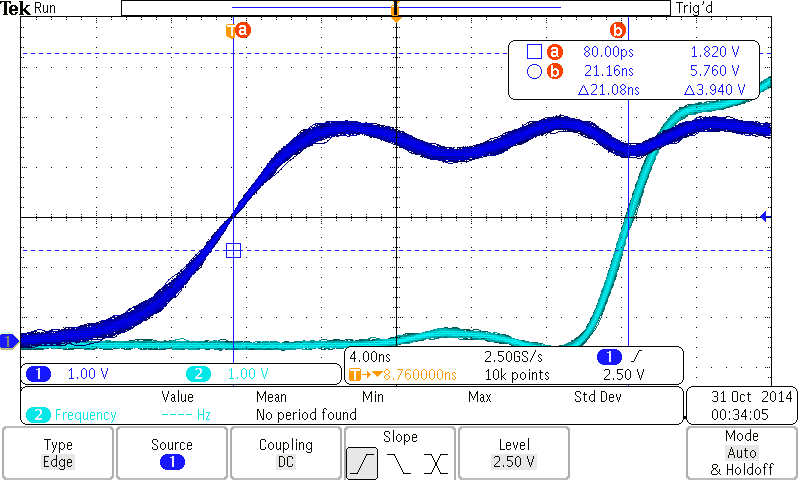


The propagation delay for falling signal is 11.64 ns.



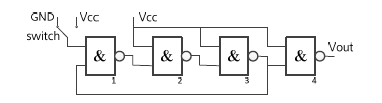
The propagation delay for of rising and falling delays are not equal, but difference between them is just 0.6 ns.

**Lab Task 2.2**

****

Propagation delay of whole circuit is 21.08ns. It is different from propagation delay of one NAND gate because whole circuit includes several NAND gates connected in parallel.

**Lab Task 3**

****

1. Input of the first NAND2 gate is in position GND.

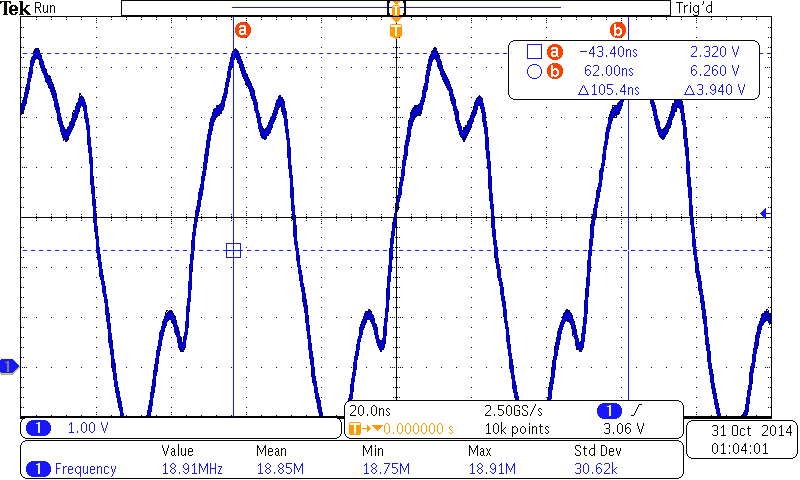
One input of first NAND2 gate connected to GDN and another to the output of 3rd NAND2 gate.

Result of 3rd NAND2 gate does not affect the Vout. And Vout is always HIGH (1).

1. Input of the first NAND2 gate is in position Vcc.

Depending on the output of 3rd NAND2 gate Vout will change. If output of 3rd NAND2 gate is HIGH (1) Vout will be HIGH (1). If output of 3rd NAND2 gate is LOW (0) Vout will be LOW (0).

So, Depending on the output of 3rd NAND2 gate Vout will oscilate.



Lab Task 4.

